REMARKS

After entry of this amendment, claims 1, 3-13, and 15-29 are pending. In the present Office Action, claims 1, 3-13, and 15-29 were rejected under 35 U.S.C. § 112, second paragraph. Claims 1, 3-11, 13, 15-21, and 23-29 were rejected under 35 U.S.C. § 102(b) as being anticipated by Tran, U.S. Patent No. 6,016,533 ("Tran"). Claims 12 and 22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tran in view of Wickeraad et al., U.S. Patent No. 6,490,654 ("Wickeraad"). Applicants respectfully traverse these rejections and request reconsideration.

Section 112 Rejection

The Office Action rejected the claims for the phrase "the first value comprising/comprises the plurality of bits," stating that it is unclear whether the plurality of bits refers to one of the pluralities of bits associated with the plurality of values, or some other plurality of bits. Applicants have amended the independent claims to recite that the first value comprising/comprises a second plurality of bits. Applicants respectfully submit that the amendment overcomes the rejection. **Because the amendment simplifies the issues for appeal by overcoming the section 112 rejection, Applicants respectfully request that the amendment be entered.**

Art Rejections

Applicants respectfully submit that claims 1, 3-13, and 15-29 recite combinations of features not taught or suggested in the cited art. For example, claim 1 recites a combination of features including: "each value of the plurality of values comprises a plurality of bits, and wherein each value is associated with a different corresponding cache line stored in the cache in a respective way of the plurality of ways, and wherein the different corresponding cache line is stored in the set selected by the decoder."

The Office Action asserts that Tran anticipates the plurality of values, citing the outputs of the multiplexors 78A-78N. See, e.g., Office Action, page 5. Applicants respectfully submit that the way prediction taught by Tran does not teach or suggest a plurality of bits forming a value that is associated with a corresponding cache line stored

in a respective way in the set selected by the decoder. For example, Tran teaches: "As depicted in FIG. 4, each storage location corresponds to a particular memory location within data array 50. For example the fifth storage location (R0, W1) within way prediction array 64 is associated with the memory location located at the intersection of physical column 0 and physical row 1 within data array 50. That memory location (R0, W1) is associated with the tag in tag array 70 stored at the intersection of row 0 and way 1. As used herein, the term memory location refers to a memory structure capable of storing a cache line. Way predictions are stored within way prediction array 64 in order relative to logical row and logical way in a one-hot encoded format. Thus each storage location stores a single bit." (Tran, col. 13, lines 33-45). Thus, the value associated with a cache line in Tran is a single bit, which does not anticipate a plurality of bits.

The Office Action responds to this argument, asserting that each value is interpreted as being the set of all values output by the multiplexors for a given way (e.g. the first value would be the bits output from multiplexors 78A, 78E, etc.). See Office Action, page 2, item 3. However, such an interpretation would then fail to anticipate that each (mulitbit) value corresponds to a different cache line. The bit output by multiplexor 78E, for example, corresponds to the cache line in way 0 of row 4, 5, 6, or 7. That cache line is not the same cache line as the cache line that corresponds to the output of the multiplexor 78A. As discussed above, every way prediction output by one of the multiplexors 78 is a single bit, and corresponds to a different cache line. Therefore, **the combination of these bits cannot form a multibit value that is associated with a different cache line from other values, since the bits themselves all correspond to different cache lines**. The combination of these vits would not form a value corresponding to a cache line, but would rather be a collection of independent bits.

Furthermore, claim 1 recites "a circuit coupled to receive the plurality of values and a first value corresponding to the first address and the first value comprising a second plurality of bits, wherein the circuit compares the first value to the plurality of values during use." The Office Action asserts that Tran anticipates the above features, citing that AND gates in figure 5 and decode[0] as the first value. Again, decode[0] is a single

bit and does not anticipate "the first value comprising the plurality of bits, wherein the circuit compares the first value to the plurality of values [each comprising a plurality of bits and each corresponding to a different cache line]."

The Office Action responds to the above argument, stating that decode[0] is compared to way 0 predictions, decode[1] is compared to way 1 predictions, etc. See Office Action, page 2, item 4. For similar reasons to those given above, Applicants respectfully submit that these bits corresponding to different cache lines cannot be combined together and be interpreted as corresponding to a given cache line.

Furthermore, the features of claim 1 would not be obvious over Tran. The use of a single way prediction bit per cache line in Tran is crucial to the operation of Tran's cache. One would not be motivated to somehow adapt Tran to use a plurality of bits of way prediction per cache line.

For at least the above stated reasons, Applicants submit that claim 1 is patentable over the cited art. Claims 3-12 depend from claim 1 and recite additional combinations of features not taught or suggested in the cited art. Claims 13 and 23 recite combinations of features including features similar to those highlighted above. Accordingly, claims 13 and 23 are also patentable over the cited art. Claims 15-22 depend from claim 13 and recite additional combinations of features not taught or suggested in the cited art. Claims 24-29 depend from claim 23 and recite additional combinations of features not taught or suggested in the cited art.

For example, claim 3 recites a combination of features including: "the circuit, if none of the plurality of values matches the first value, asserts an early miss signal during use, wherein the early miss signal indicates that the first address is a miss in the cache prior to a tag comparison between the first address and the plurality of tags." By contrast, Tran can only detect a cache miss via the tag comparisons (see, e.g., Tran, col. 13, lines 16-21 and col. 15, lines 28-40). Applicants reserve the right to highlight additional distinctions in the dependent claims if the case proceeds to Appeal.

The Office Action responds to this argument, asserting that in the case that an address is a miss and is then accessed again, it would be the case that the Tang [sic] discloses a miss prior to performing a tag comparison. Applicants respectfully disagree with this interpretation. Nevertheless, even under this interpretation, the first address was compared during the first access as well. Accordingly, there is no early miss that occurs before the first address is compared, since it has already been compared (during the first access) when the second access occurs.

CONCLUSION

Applicants submit that the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/6363-00600/LJM.

Respectfully submitted,

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